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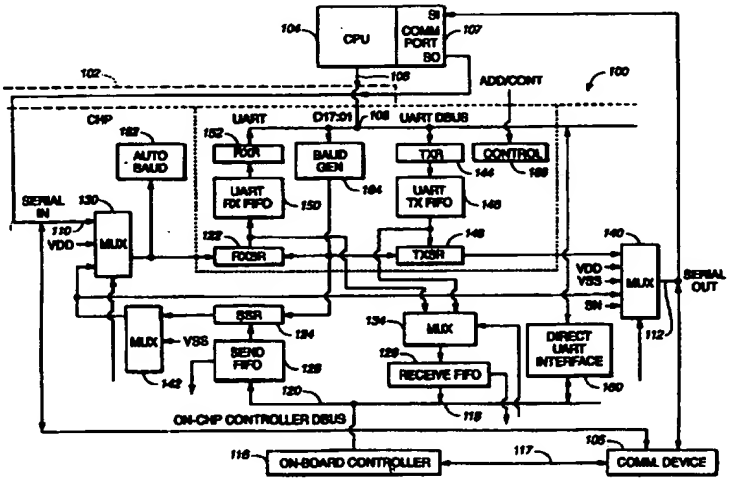

(57) Abstract

The present invention is directed to a method and apparatus for interfacing asynchronous communications wherein an on-board controller can further monitor and/or process data being transferred without degrading overall system throughput. In accordance with exemplary embodiments, such a feature is achieved by providing means (126, 128) for buffering data on both a receive and send side of an on-board controller (116) included within an asynchronous communications device (105). Exemplary embodiments of the present invention provide this capacity without affecting universal applicability of the asynchronous communications device (105) as either a serial-to-serial interface, a parallel-to-parallel interface or as a serial-to-parallel interface (or vice versa). For example, regardless of whether the asynchronous communications device serves as an interface to a first device operating in a serial mode or in a parallel mode, an on-board controller (116) is provided which can monitor and/or process the data being transferred from or received by the first device.

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METHOD AND APPARATUS FOR INTERFACING DEVICES USED IN ASYNCHRONOUS COMMUNICATIONS

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates generally to data communications methods and systems, and more particularly, to a method and apparatus for interfacing devices used in connection with asynchronous communications.

State of the Art:

The use of interface elements for accommodating asynchronous communications between devices is well known. For example, U.S. Patent No. 4,823,312 (Michael et al) describes an asynchronous communications element.

More particularly, the Michael patent discloses an asynchronous communications element which is located between a central processing unit (CPU) configured for parallel transmission and receipt of data and a communications station configured for serial transmission and receipt of data. The asynchronous communications device therefore serves to interface bidirectional communications between the CPU and the communications station. To reduce CPU interrupt overhead, the asynchronous communications element includes a transmitter first-in first-out (FIFO) memory as a buffer for data which is to be transmitted from the CPU to the communications station. A receiver FIFO is used as a receive buffer for data transfers from the communications station to the CPU.

The receiver FIFO receives data of a data transfer from the communications station to the CPU via a receiver shift register. Data which is received by the receiver shift register is transferred in parallel to the receiver FIFO which, after buffering one or more such data transfers, supplies the data to the CPU. Because a plurality of data transfers can be buffered in the receiver FIFO before being transferred to the CPU, the CPU interrupt overhead can be reduced.

Similarly, one or more data transfers from the CPU to the communications station can be buffered in the transmitter FIFO. The transmitter FIFO can then

sequentially transfer the data to a transmitter shift register, which transfers the data in series to the communications station.

Despite the known use of FIFOs to buffer data in conventional asynchronous communications elements, these FIFOs can limit functionality of the communications element. For example, the FIFOs of conventional asynchronous communications elements, such as that described in the Michael patent, are provided only for the benefit of the CPU. That is, these FIFOs merely buffer bidirectional data transfers to and from the CPU and therefore only reduce interrupt overhead of the CPU. Consequently, conventional asynchronous communications elements cannot exploit the processing power of any con-troller included in the asynchronous communications element as a supplement to processing power of the CPU or the communications station without seriously degrading overall data throughput.

Therefore, any controller included within the asynchronous communications element, for all practical purposes, is prohibited from monitoring and/or further processing the data which is transferred between the CPU and the communications station. If a controller within the asynchronous communications element were provided the capability to process data transferred between the CPU and the communications station, interrupt overhead of the controller in the asynchronous communications element would increase and thereby significantly degrade overall data throughput.

A further drawback of conventional asynchronous communications elements it that they must be configured in advance as either a serial interface or a parallel interface for the CPU, and any software implemented by the communications element must be adapted to that configuration. For example, in the embodiment described in the Michael patent, the asynchronous communications element is configured to transfer serial data from the communications station to the CPU in parallel and to transfer parallel data from the CPU to the communications station in series. An on-board controller of the asynchronous communications element is programmed accordingly. Thus, if the CPU is later configured with a built-in serial input/output communications port, the asynchronous communications element

along with any control software must be reconfigured to properly function as a serial-to-serial interface for asynchronous data.

Accordingly, it would be desirable to overcome drawbacks of conventional asynchronous communications elements such as that described in the Michael patent. More particularly, it would be desirable to provide an asynchronous communications element which can exploit the capabilities of an on-board controller included within the asynchronous communications element to provide further monitoring and/or processing of data being transferred without degrading overall system throughput. In addition, it would be desirable to provide an asynchronous communications element which, in addition to being universally adaptable to different data rates, is also adaptable to either function as a parallel-to-serial interface or as a serial-to-serial interface without requiring any system reconfiguration or redesign of control software for the on-board controller.

SUMMARY OF THE INVENTION

The present invention is generally directed to a method and apparatus for interfacing asynchronous communications wherein an on-board controller can further monitor and/or process data being transferred without degrading overall system throughput. In accordance with exemplary embodiments, such a feature is achieved by providing means for buffering data on both a receive and send side of an on-board controller included within an asynchronous communications device. Exemplary embodiments of the present invention provide this capability without affecting universal applicability of the asynchronous communications device as either a serial-to-serial interface, a parallel-to-parallel interface or as a serial-to-parallel interface (or vice versa). For example, regardless of whether the asynchronous communications device serves as an interface to a first device operating in a serial mode or in a parallel mode, an on-board controller is provided which can monitor and/or process the data being transferred from or received by the first device.

Generally speaking, exemplary embodiments of the present invention relate to a method and apparatus, such as an asynchronous communications device, for

transferring data between a first device and a second device. Exemplary embodiments of such an apparatus include a first input for receiving data from at least one of the first device and the second device; a first output for transferring data received via the first input to the other of said first device and said second device; and means for controlling, such as an on-board controller, transfer of data between said first device and said second device. The means for controlling, in accordance with exemplary embodiments, includes a controller input for receiving data from one of said first device and said second device; a controller output for transferring the data to the other of said first device and said second device; and means for buffering data, such as a FIFO, for at least one of receipt by said controller input and transfer from said controller output. By supplying a data buffering means for the on-board controller, the on-board controller can monitor and/or process data transferred between the first and second devices without requiring a large number of interrupts to the on-board controller which could degrade overall throughput.

Further, exemplary embodiments of the present invention relate to a method and apparatus for transferring data between a first device and a second device, the first device being operable in both a serial mode and a parallel mode, said apparatus comprising: a first input for selectively receiving data in at least one of a serial format and a parallel format from at least one of said first device and said second device; a first output for transferring data received via said first input to the other of said first device and said second device, said data being transferred in at least one of said serial format and said parallel format; and means for controlling a transfer of said data between said first device and said second device by selectively converting data of said parallel format into data of said serial format (e.g., for selective input to or output from an on-board controller) when the first device is in either a serial mode or a parallel mode of operation. Further, the means for controlling selectively converts data of said serial format into data of said parallel format (e.g., for selective input to or output from the on-board controller). Thus, to provide an ability of the on-board controller to monitor and/or process data in both serial and parallel modes of operation of the first

and/or second device, exemplary embodiments of a controlling means include a controller input for receiving data from said first device during a serial mode of operation and during a parallel mode of operation; and a controller output for transferring data to said first device during said serial mode of operation and during said parallel mode of operation.

BRIEF DESCRIPTION OF THE DRAWING

The present invention can be further understood with reference to the following description and the appended drawing, wherein:

Figure 1 is an exemplary block diagram of an asynchronous communications device in accordance with an exemplary embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 illustrates an exemplary embodiment of an apparatus, such as an asynchronous communications device, for transferring data between a first device and a second device in accordance with the present invention. Each of the first and second devices can, for example, be a computer, such as any personal computer, or other device which is capable of sending and receiving data. Both the first and second devices are connected to the data transfer apparatus via any communication path, such as any wired communication path (e.g., telephone line), or wireless communication path. For purposes of the following discussion, the data transfer apparatus will be described in the context of an asynchronous communications device which is capable of interfacing a first device to one or more second devices for both synchronous and asynchronous data transfer. Further, the communication path will be described in the context of a serial path. However, a parallel path can also be used if desired.

The Figure 1 apparatus can be considered to provide functions typically associated with an asynchronous communications device, such as that described in the Michael patent, the disclosure of which is hereby incorporated by reference in its entirety. However, exemplary embodiments of the present invention further

provide an ability to use an on-board controller of the asynchronous communications device to provide additional functionality without significantly increasing the number of interrupts to the on-board controller and without significantly degrading throughput of data transfers between devices connected to one another via the asynchronous communications device. Further, exemplary embodiments of an asynchronous communications device can provide a common architecture and mode of operation for interfacing the first device to one or more second devices, regardless of whether the first device is configured for a serial mode of data transfer or a parallel mode of data transfer.

In accordance with exemplary embodiments, the term "data" constitutes information of any sort which is transferred from one device to another. Thus, data can include information representing numerical values, text, commands, status information or any other information that can be transmitted in any form between two devices.

Referring to the exemplary Figure 1 embodiment, the asynchronous communications device is labeled 100, and includes a first input 102 for receiving data from at least one of the first device and the second device. The first input, in accordance with exemplary embodiments, can selectively receive data in at least one of a serial format and a parallel format from at least one of the first device and the second device.

For purposes of the following discussion, the exemplary Figure 1 embodiment will be described in the context of providing full duplex communications between a computer 104 and a communications device 105 (such as a data pump). Further, to simplify the following discussion, the exemplary Figure 1 embodiment will be described in the context of an asynchronous communications device 100 which monitors data transfers sent from or received by the computer 104 when computer 104 operates in either a parallel mode or a serial mode.

Data transfers sent from the computer 104 which have been processed by an on-board controller 116 of the asynchronous communications element 100 can then be transferred from the on-board controller directly to the communications

device 105 via parallel signal lines 117 which interconnect the on-board controller 116 and the communications device 105. Similarly, data transfers from the communications device 105 can be received by the on-board controller 116 via parallel signal lines 117; the data can then be processed by the on-board controller 116 and forwarded to the computer 104. Although these data transfers will be described to illustrate features of the present invention, those skilled in the art will appreciate that the invention is not so limited. For example, those skilled in the art will appreciate that rather than directly coupling the on-board controller 116 and the communications device 105 via parallel signal lines 117, all communications between these devices can be performed via buffered paths of the asynchronous communications element to be described herein, with each of the computer 104 and the communications device 105 communicating either serial data or parallel data.

As mentioned above, the first device is a communications device represented as computer 104 of Figure 1 which can be configured in either a parallel mode of operation or in a serial mode of operation. In either case, the input/output of the computer 104 is connected to a second device, represented in Figure 1 as communications device 105, via the asynchronous communications device 100. For purposes of simplifying the following discussion, the "first device" will be used to reference computer 104, while the "second device" will be used to reference communications device 105. Of course, those skilled in the art will appreciate that the communications device 105 can be considered the first device and the computer 104 can be considered the second device. To illustrate features of the invention, both a parallel mode of operation and a serial mode of operation for the computer 104 will be described.

In a parallel mode of operation, an internal databus of the computer 104 is directly connected to a databus of the asynchronous communications device 100. In the exemplary Figure 1 embodiment, the databus 106 is illustrated as an 8-bit bus. However, those skilled in the art will appreciate that a databus of any size can be used in accordance with exemplary embodiments of the present invention.

To illustrate the computer 104 being configured for a serial mode of operation, a communications port, such as communications port 107, is provided. In this case, the asynchronous communications device 100 interfaces with the serial input/output of the communications port.

Where the asynchronous communications device 100 monitors and/or further processes data transferred from the computer 104 to communications device 105, as well as data received from communications device 105, the computer 104 transmits data to and receives data from the second device via the asynchronous communications device 100 in both a parallel mode of operation and in a serial mode of operation. To accommodate both modes of operation, the first input 102 of the asynchronous communications device includes both a parallel input/output 108 and a serial input 110 for interfacing the computer 104 with the asynchronous communications device. Data from computer 104 can be monitored and/or processed by the asynchronous communications device and then sent to the communications device 105 from the on-board controller 116 via parallel signal lines 117. Data received from the communications device 105 via parallel signal lines 117 can be monitored and/or processed by the on-board controller 116 and then sent to the computer 104 via a first output of the asynchronous communications device which includes the parallel input/output 108 and a serial output 112. The serial output 112 supplies serial data to computer 104 via the serial input of the communication port 107.

An overview of the input of data to computer 104 from communications device 105 in both a parallel mode and a serial mode will now be provided. To input data to computer 104 in a parallel mode of operation, the input/output 108 is interfaced to databus 106 for parallel connection directly to the internal databus of the computer 104. Thus, data received from the second device can be processed in the asynchronous communications element 100 and then forwarded directly to the internal bus of computer 104.

In a serial mode of operation, data can be transferred from the communications device 105 to the serial input 102 of the communications port 107, and serial-to-parallel conversion is unnecessary. However, in accordance with

exemplary embodiments, parallel data is supplied from communications device 105 to the asynchronous communications device 100, wherein the data is monitored by the on-board controller and then sent to the serial input of the serial interface 107.

Data can also be transmitted from computer 104 to the communications device 105 in either a serial mode of operation or a parallel mode of operation. In both modes, the data can be monitored and/or processed by the on-board controller. More particularly, although serial data output from the communications port can be directly supplied to the serial communications path which interconnects computer 104 and communications device 105, exemplary embodiments provide a path for this data through the asynchronous communications device 100 such that the data can be monitored and/or further processed.

To permit on-board monitoring of the data by the asynchronous communications device when computer 104 operates in a serial mode, it can be supplied from computer 104 to the serial input 110. In accordance with exemplary embodiments, serial data which is supplied from the communications port 107 of computer 104 to the serial input 110 is parallelized within an internal data path of the asynchronous communications device so that it can be monitored by the on-board controller 116. After being monitored and/or further processed by the on-board controller, the data can sent in a parallel format to the communications device 105 via parallel signal lines 117. Of course, in alternate embodiments, the data monitored and/or processed by the on-board controller 116 can again be serialized and then forwarded via the serial output 112 to the communications device 105.

Where the computer 104 sends data in a parallel mode, data is supplied to the asynchronous communications device via its parallel input/output 108. The data can then be processed within the asynchronous communications element and forwarded to the communications element 105 via the parallel signal lines 117. Again, as with the serial mode, data monitored and/or processed by the on-board controller in the parallel mode can, in an alternate embodiment, be serialized for transmission to the communications device 105. Thus, data can be transferred to the communications device 105 in either a serial format or a parallel format.

To accommodate the foregoing operation, the asynchronous communications device 100 includes a first output for transferring data received via the first input to the other of the first device and the second device. Where the first device is the computer 104 described previously, the output can be a connection to a communication path (e.g., telephone line) that is in turn connected to the second device.

Those skilled in the art will, of course, appreciate that the devices designated as the first and second devices can be reversed. Further, as with the case where data transmitted by computer 104 is monitored by the asynchronous communications device in both parallel and serial modes of operation, data transmitted from the second device for receipt by computer 104 can also be monitored in both parallel and serial modes of operation.

Thus, exemplary embodiments of the present invention can accommodate synchronous and asynchronous communications between a first device and a second device, regardless of whether either or both of the first and second devices are configured for a parallel mode of operation or for a serial mode of operation. Further, in accordance with exemplary embodiments of the present invention, regardless of whether the asynchronous communications device is accommodating a parallel data transfer or a serial data transfer, an on-board control means included within the asynchronous communications device can process any data which is being transmitted or received.

The monitoring and/or processing performed by the on-board controller of asynchronous communications device 100 can be specified by the user. For example, where the computer 104 is to transfer data to communications device 105 via the asynchronous communications device 100, it may be desirable to compress (or decompress) the data before transmission. Alternately, where serial data is received by the asynchronous communications device in compressed (decompressed) format from the second device, it may be desirable for the on-board controller of the asynchronous communications device to decompress (compress) this data before it is forwarded to the computer 104.

In accordance with exemplary embodiments, an on-board controller of the asynchronous communications device can provide this compress/ decompress functionality. For this purpose, exemplary embodiments of an on-board control means included within the asynchronous communications device 100 monitor all data transfers regardless of their format.

More particularly, the asynchronous communications device of Figure 1 includes a means for controlling a transfer of data between the first device and the second device. The controlling means is represented in the Figure 1 example as an on-board controller 116. Of course, those skilled in the art will appreciate that the controller of the asynchronous communications device need not be formed on a single chip with other components of the asynchronous communications device, but rather can be formed with one or more components of the asynchronous communications device in one or more chips.

In accordance with exemplary embodiments, the on-board controller controls a transfer of data between the first device and the second device by selectively converting data of parallel format into data of serial format, and by converting data of serial format into data of parallel format. For example, as described previously, when computer 104 is in a parallel mode, parallel data from the internal bus of the computer 104 can be directly output to the communications device or, alternately, can be supplied to the on-board controller for monitoring and/or further processing. Afterwards, the parallel data output from the on-board controller can be supplied to the communications device 105 via parallel signal lines 117. Alternately, with appropriate interfacing, the parallel data can be serialized within the asynchronous communications element after being processed by the on-board controller 116, and then supplied to communications device 105 in a serial format.

Further, when computer 104 is in a parallel mode, data received by the computer 104 from communications device 105 via the serial input 110 can be parallelized and then supplied to the databus 106. Alternately, the serial data received can be parallelized and then monitored and/or further processed by the on-board controller before being forwarded to databus 106. Of course, parallel

data received from the communications device 105 can also be monitored and/or processed by the asynchronous communications element and then sent to the computer 104.

Where the computer 104 is in a serial mode of operation, data from the second device can be supplied directly to the communications port of computer 104. Alternately, the data can be supplied via the serial input 110 of the asynchronous communications device, wherein it can be parallelized for monitoring and/or further processing by the on-board controller. Alternately, parallel data from the communications device 105 can be received by the on-board controller 116 via the parallel signal lines 117. Afterwards, the output from the on-board controller can be serialized and forwarded via serial output 112 to the communications port 107 of computer 104.

Similarly, with appropriate interfacing, data transmitted by computer 104 in a serial mode can be supplied directly via the serial output of the communications port to the communications device 105, or it can be parallelized within the asynchronous communications device for input to the on-board controller. After being monitored and/or further processed by the on-board controller, the data can be serialized and supplied via output 112 to communications device 105, or alternately, can be supplied directly from the on-board controller to the communications device 105 via the parallel signal lines 117.

Thus, in accordance with exemplary embodiments, all data transmitted by computer 104 or received from the second device can be selectively converted to a parallel format for monitoring and/or processing by the on-board controller. For this purpose, the on-board controller includes a controller input 118 for receiving data from one of the first device and the second device. For example, the on-board controller receives data which is being transferred by the computer 104 via the databus 106 or via the serial output of communications port 107. In alternate embodiments, with appropriate interfacing, the on-board controller can also receive serial data from the communications device 105 via controller input 118. The serial data can be parallelized and then sent to the computer 104 via the controller input 118 and the controller 116. In addition to controller input 118, the controller

includes a controller output 120 for transferring data to the other of the first and the second device after it has been monitored and/or processed by the on-board controller.

Those skilled in the art will appreciate that exemplary embodiments of an asynchronous communications device in accordance with the present invention, such as that illustrated in Figure 1, can therefore provide asynchronous data transfer regardless of whether data is transferred in a serial format or a parallel format. Further, the on-board controller of the asynchronous communications device can be used to implement additional functionality associated with monitoring and/or further processing any or all data transferred through the asynchronous communications device, regardless of whether the data is received by the asynchronous communication device in a parallel format or in a serial format.

The ability to process data, regardless of whether it is received in a serial format or in a parallel format, avoids any need to reconfigure the internal structure of the asynchronous communications device to accommodate a parallel mode of operation or a serial mode of operation. Further, there is no need to develop separate software control for parallel and serial modes of operation, respectively. Rather, external devices need merely be connected to the appropriate inputs of the asynchronous communications device to achieve desired data transfer.

To exploit functionality of the on-board controller without affecting interrupt overhead of the on-board controller, exemplary embodiments further include means for buffering data for at least one of receipt by the on-board controller and transmission by the on-board controller. That is, any data to be monitored and/or processed by the on-board controller is buffered via at least one of a receive FIFO 126 of the controller input and a send FIFO 128 of the controller output. The buffers can store any number of data transfers and, in an exemplary embodiment, each store four bytes of data. These buffers can, in an exemplary embodiment, be configured and monitored by the on-board controller. As a result, the number of interrupts necessary to process data by the on-board

controller can be significantly reduced to thereby enhance overall system throughput.

For example, where data supplied from computer 104 is to be compressed by the asynchronous communications device before being sent to a communications path connected with an output of the asynchronous communications device, the data can be parallelized, if necessary and then buffered in the receive FIFO 126. When all data associated with a given data transfer has been buffered, or when the receive FIFO is full, a single interrupt can be generated to the on-board controller so that all such data can be compressed at once. After monitoring and/or processing, the data can be transferred to the communications device 105 via the parallel signal lines 117, or, if appropriate interfacing is provided, can be sent via the serial output 112.

Where data has been processed by the on-board controller, a single interrupt of the on-board controller will result in the processed data being buffered in the send FIFO 128. The use of the send FIFO avoids the need for the on-board controller to monitor the status of any output register associated with, for example, serializing of the processed data, and therefore reduces the number of controller interrupts associated with outputting data from the on-board controller. Those skilled in the art will appreciate that the send FIFO is not used when data has been sent to the on-board controller 116 from computer 104 for subsequent transfer to the communications device 105 via parallel signal lines 117.

Having described exemplary embodiments of the present invention with respect to Figure 1, a more detailed discussion will now be provided of the various data paths through the exemplary asynchronous communications device of Figure 1 for both parallel and serial operation modes of computer 104. In accordance with exemplary embodiments described herein, it will be presumed that data is received from the communications device 105 via parallel signal lines 117 and on-board controller 116. Further, it will be presumed that data is sent by computer 104 via the on-board controller 116 and parallel signal lines 117. However, as described previously, alternate exemplary embodiments, if configured with appropriate interfacing, can send and receive data using serial output 112 and

serial input 110, respectively. Thus, the following data paths will be described with respect to the exemplary Figure 1 embodiment:

(1) Transmission of data by first device in a serial mode;

(2) Receipt of data by first device in serial mode;

(3) Transmission of data by first device in parallel mode; and

(4) Receipt of data by first device in parallel mode.

(1) Transmission of data by first device in serial mode

Data is transferred from the computer 104 during a serial mode of operation via the serial output of communications port 107. With appropriate interfacing the serial output from the communications port can be optionally supplied directly to the communications device 105. The interfacing would be required to ensure that the computer 104 and the communications device 105 can determine where data is being communicated to and where data is being communicated from during, for example, half or full duplex communication. Such interfacing can, for example, include the use of multiplexers and/or dedicated signal lines between the computer 104, the asynchronous communications device 100 and the communications device 105.

In accordance with exemplary embodiments, data transferred via the serial output of communications port 107 can also be monitored and/or further processed by the on-board controller 116. Accordingly, the serial output from the communications port is supplied via serial input 110 to the asynchronous communications device. The serial data supplied from computer 104 is directed via a multiplexer 130 which, in turn, is connected to the receive shift register 122. The receive shift register converts the serial data from the computer 104 into parallel data which can be supplied via a multiplexer 134 to the receive FIFO 126. As mentioned previously, the receive FIFO can be used to buffer one or more serial data transfers from the computer 104 so that only a single interrupt to the on-board controller 116 is necessary for supplying the one or more data transfers to the on-board controller. The on-

board controller can then perform any desired monitoring and/or co-processing of the data, such as compression.

After the data has been monitored and/or further processed (e.g., compressed) by the on-board controller, it can be supplied via signal line 117 to the communications device 105. Alternately, the data of one or more data transfers can be downloaded from the on-board controller, via a single interrupt, to the send FIFO 128. The data buffered in send FIFO 128 can then be sequentially serialized via a send shift register 124. Once serialized, the data can be supplied to the serial output 112 of the asynchronous communications element via multiplexers 142 and 140 provided appropriate interfacing is provided.

(2) Receipt of data by first device in serial mode

To receive data during a serial mode, serial data on the communications path (e.g., phone line) can be optionally supplied directly to the serial input of the communication port 107 of the computer 104 with appropriate interfacing. Because, in the exemplary embodiment illustrated on Figure 1, a phone line is typically considered a serial data path, a parallel-to-serial conversion would be unnecessary for input to the serial input of the communication port.

However, because the asynchronous communications device 100 monitors all data transmitted or received by the computer 104 in accordance with an exemplary embodiment described herein, the data from the second device can also be received by the on-board controller 116 in parallel format via parallel signal line 117. Alternately, the data can be supplied from the second device via the serial input 110 and a multiplexer 130 to the receive shift register 122 wherein the serial data is converted into parallel data. The parallel data from the receive shift register can then be supplied via multiplexer 134 to the receive FIFO 126, wherein data of one or more data transactions can be buffered before being processed (e.g., decompressed) by the on-board controller.

After monitoring and/or further processing by the on-board controller, the data received from the communications device 105 can be buffered in send FIFO 128 before being serialized in send shift register 124. As data is sequentially serialized, it can be forwarded to the communications port 107 of computer 104 via multiplexers 142 and 140.

Having described the serial mode of operation, a discussion of a parallel mode of operation of computer 104 will now be discussed.

(3) Transmission of data by first device in parallel mode

In a parallel mode during which data is transmitted from computer 104, data is supplied by the computer directly to its internal bus. The data from the internal bus is forwarded directly to the data bus 106 and into a transmitter register 144. From the transmitter register 144, the data is buffered in a conventional transmit FIFO 146.

With appropriate interfacing, the buffered data from the transmit FIFO 146 can then be serialized via a transmitter shift register 148 and supplied to serial output 112 via multiplexer 140. Alternately, the data buffered in FIFO 146 can be supplied via multiplexer 134 to the receive FIFO 126 of the on-board controller. Plural data transfers can be buffered in the receive FIFO 126 and then downloaded to the on-board controller using a reduced number of interrupts (e.g., a single interrupt if the receive FIFO does not overflow). As a result, data transmitted by the computer 104 can be processed by the on-board controller (e.g., compressed).

After being monitored and/or processed by the on-board controller 116, the data can be output from the asynchronous communications device directly to the communications device 105 via parallel signal lines 117. Alternately, the data can be output from the asynchronous communications device via send FIFO 128, send shift register 124, and multiplexers 142 and 140, provided appropriate interfacing (for example, additional communication lines) is provided between the computer 104, the asynchronous

communications device 100 and the communications device 105 to accommodate half or full duplex operation.

(4) Receipt of data by first device in parallel mode

The receipt of data by computer 104, when computer 104 is in a parallel mode of operation is performed as follows. With appropriate interfacing between the computer 104, the asynchronous communications device 100 and the communications device 105, serial data can be optionally supplied directly by the second device via the phone line, the serial input 110 and multiplexer 130 to the receiver shift register 122. Recall that the receiver shift register 122 parallelizes the data, with data of one or more transactions being buffered in a conventional receive FIFO 150. The one or more data transfers buffered in the receive FIFO can then be transferred via a receiver register 152 directly to the internal bus of the computer 104 via data bus 106.

Alternately, to provide the capability for the on-board controller to monitor and/or further process incoming data, the data can be routed to the on-board controller. As a result, the on-board controller can process (e.g., decompress) any incoming data, if necessary, before it is supplied to the computer 104.

To provide a monitoring and/or processing capability via the on-board controller, parallel data from communications device 105 can be supplied via parallel signal lines 117 to the on-board controller 116. Alternately, with appropriate interfacing, data which has been received via the phone line can be supplied via multiplexer 130, receive shift register 122 and receive FIFO 126 to the on-board controller 116 where it can be processed (e.g., decompressed).

Once processed, the data can be output from the on-board controller to the internal bus of computer 104 via send FIFO 128. Because the computer 104 is in a parallel mode, the data is supplied from the on-board controller via

the send FIFO 128 to the send shift register 124 which converts the parallel data output from the on-board controller into serial data. The serial output of the send shift register 124 can then be supplied via the multiplexers 142 and 130 to the receiver shift register 122 which again parallelizes the data. The parallel output of the receiver shift register 122 can be buffered in receiver FIFO 150 and then supplied to the parallel lines of the databus in computer 104 via receiver register 152 and databus 106.

Of course, those skilled in the art will appreciate that the present invention is not limited to the exemplary embodiments described with respect to Figure 1, and variations of the Figure 1 embodiment as described previously would be readily apparent to those skilled in the art. Further, additional variations of the Figure 1 embodiment which have not been set forth specifically will be apparent to those skilled in the art. For example, when data is to be received by the computer 104 in a parallel mode of operation, routing of the parallelized data output from the send FIFO 128 can be supplied directly to the receiver FIFO 150 through a data path which does not include the send shift register 124 and the receive shift register 122. Such an alternate path would avoid the parallel-to-serial conversion followed by a serial-to-parallel conversion.

Further, those skilled in the art will appreciate that to provide a selective bypass of either serial input/output or parallel input/output of data between the computer 104 and the communication device 105, appropriate interfacing such as interface multiplexers, can be connected to the various input/output lines of these devices. As a result, the user can selectively configure the communications system to eliminate any monitoring and/or processing of data by the asynchronous communications device 100.

In addition, those skilled in the art will appreciate that a direct interface between the computer 104 and the on-board controller 116 can be provided. For example, a direct interface 160 can be provided such that data can be transferred between the computer 104 and the on-board controller selectively, without requiring that the information be buffered in either the

conventional receiver and transmitter FIFOs 150, 146 of a conventional universal asynchronous receiver/transmitter communications element, and without transmission of the data through the send and receive FIFOs 128, 126 of the Figure 1 asynchronous communications device. This feature can, for example, be used by the on-board controller to access registers connected to a conventional databus of the universal asynchronous receiver/transmitter in Figure 1 (e.g., during initialization) over the same bus used by the computer 104 to access these registers. These registers can include conventional registers used for data interface, monitoring capability and control. Arbitration logic is unnecessary in controlling access to these registers in an exemplary embodiment; rather when the computer 104 is active, the direct UART interface is disabled.

The foregoing description of exemplary embodiments has focused on elements which are directed to inventive features of the present invention, and other elements which are conventional and known to those skilled in the art have not been described in great detail. However, those skilled in the art will appreciate that any conventional features of a universal asynchronous receiver/transmitter communications device can be incorporated into an asynchronous communications device in accordance with exemplary embodiments of the present invention.

For example, a hardware autobaud block 162 can be provided for a serial mode of operation to automatically detect and set an incoming band rate. Similarly, the asynchronous communications device can include a baud generator 164 similar to that described in the Michael patent. Further, control registers 166 similar to control registers and control logic described with respect to the Michael patent can be included to provide conventional universal asynchronous receiver/transmitter functions. Further, signal lines illustrated and/or described as parallel signal lines or as serial signal lines are by way of example only. Those skilled in the art will appreciate that any or all of the signal lines can be configured as serial, parallel or any combination of serial and parallel signal lines.

It will be appreciated by those skilled in the art that the present invention can be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The presently disclosed embodiments are therefore considered in all respects to be illustrative and not restricted. The scope of the invention is indicated by the appended claims rather than the foregoing description and all changes that come within the meaning and range and equivalence thereof are intended to be embraced therein.

WHAT IS CLAIMED IS:

1. Apparatus for transferring data between a first device and a second device comprising:

a first input for receiving data from at least one of said first device and said second device;

a first output for transferring data received via the first input to the other of said first device and said second device;

means for controlling a transfer of data between said first device and said second device, said means for controlling further including:

a controller input for receiving data from one of said first device and said second device;

a controller output for transferring data to the other of said first device and said second device; and

means for buffering data for at least one of receipt by said controller input and transfer from said controller output.

2. Apparatus according to claim 1, wherein said first device further includes:

a computer having a databus for parallel transfer of data to said first input.

3. Apparatus according to claim 1, wherein said first device further includes:

a computer having a communications port for serial transfer of data to said first input.

4. Apparatus according to claim 1, wherein said first device further includes:

a computer having a databus for parallel receipt of data from said first output.

5. Apparatus according to claim 1, wherein said first device further includes:

a computer having a communications port for serial receipt of data from said first output.

6. Apparatus according to claim 1, wherein said controlling means monitors data transfers between said first device and said second device.

7. Apparatus according to claim 1, wherein said controlling means processes data transferred between said first device and said second device.

8. Apparatus according to claim 7, wherein said controlling means compresses and decompresses data transferred between said first device and said second device.

9. Apparatus according to claim 1, wherein said data buffering means further includes:

at least one first-in first-out memory.

10. Apparatus according to claim 9, wherein said data buffering means further incudes:

a first FIFO for buffering data input to said controlling means; and

a second FIFO for buffering data processed by said controlling means prior to transfer of said data from said controlling means to at least one of said first device and said second device.

11. Apparatus for transferring data between a first device and a second device, the first device being operable in both a serial mode and a parallel mode, said apparatus comprising:

a first input for selectively receiving data in at least one of a serial format and a parallel format from at least one of said first device and said second device;

a first output for transferring data received via said first input to the other of said first device and said second device, said data being transferred in at least one of said serial format and said parallel format; and

means for controlling a transfer of said data between said first device and said second device by selectively converting data of said parallel format into data of said serial format and by converting data of said serial format into data of said parallel format, said controlling means further including:

a controller input for receiving data from said first device during a serial mode of operation and during a parallel mode of operation; and

a controller output for transferring data to said first device during said serial mode of operation and during said parallel mode of operation.

12. Apparatus according to claim 11, wherein said first device further includes:

a computer having a databus for parallel transfer of data to said first input, said second device being connected to said first output for serial transfer of data between said first output and said second device.

13. Apparatus according to claim 11, wherein said first input is connected for serial transfer of data from said second device, said first output being connected for parallel transfer of data to said first device.

14. Apparatus according to claim 11, wherein said controlling means further includes:

means for buffering data for at least one of receipt by said controller input and transfer from said controller output.

15. A method for transferring data between a first device and a second device comprising the steps of:

receiving data from at least one of said first device and said second device;

transferring data received to the other of said first device and said second device; and

controlling a transfer of data between said first device and said second device, said means for controlling further including:

receiving data from one of said first device and said second device; and

transferring data to the other of said first device and said second device; and

buffering data for at least one of receipt by said controller input and transfer from said controller output.

16. A method according to claim 15, further including a step of:

receiving parallel data from at least one of said first device and said second device.

17. A method according to claim 15, further including a step of:

receiving serial data from at least one of said first device and said second device.

18. A method for transferring data between a first device and a second device, the first device being operable in both a serial mode and a parallel mode, comprising the steps of:

selectively receiving data in at least one of a serial format and a parallel format from at least one of said first device and said second device;

transferring data received to the other of said first device and said second device, said data being transferred in at least one of said serial format and said parallel format; and

controlling a transfer of said data between said first device and said second device by selectively converting data of said parallel format into data of said serial format and by converting data of said serial format into data of said parallel format, said step of controlling further including:

receiving data from said first device during a serial mode of operation and during a parallel mode of operation; and

transferring data to first device during said serial mode of operation and during said parallel mode of operation.

19. A method according to claim 18, further including a step of:

receiving parallel data from at least one of said first device and said second device.

20. A method according to claim 18, further including a step of:

receiving serial data from at least one of said first device and said second device.

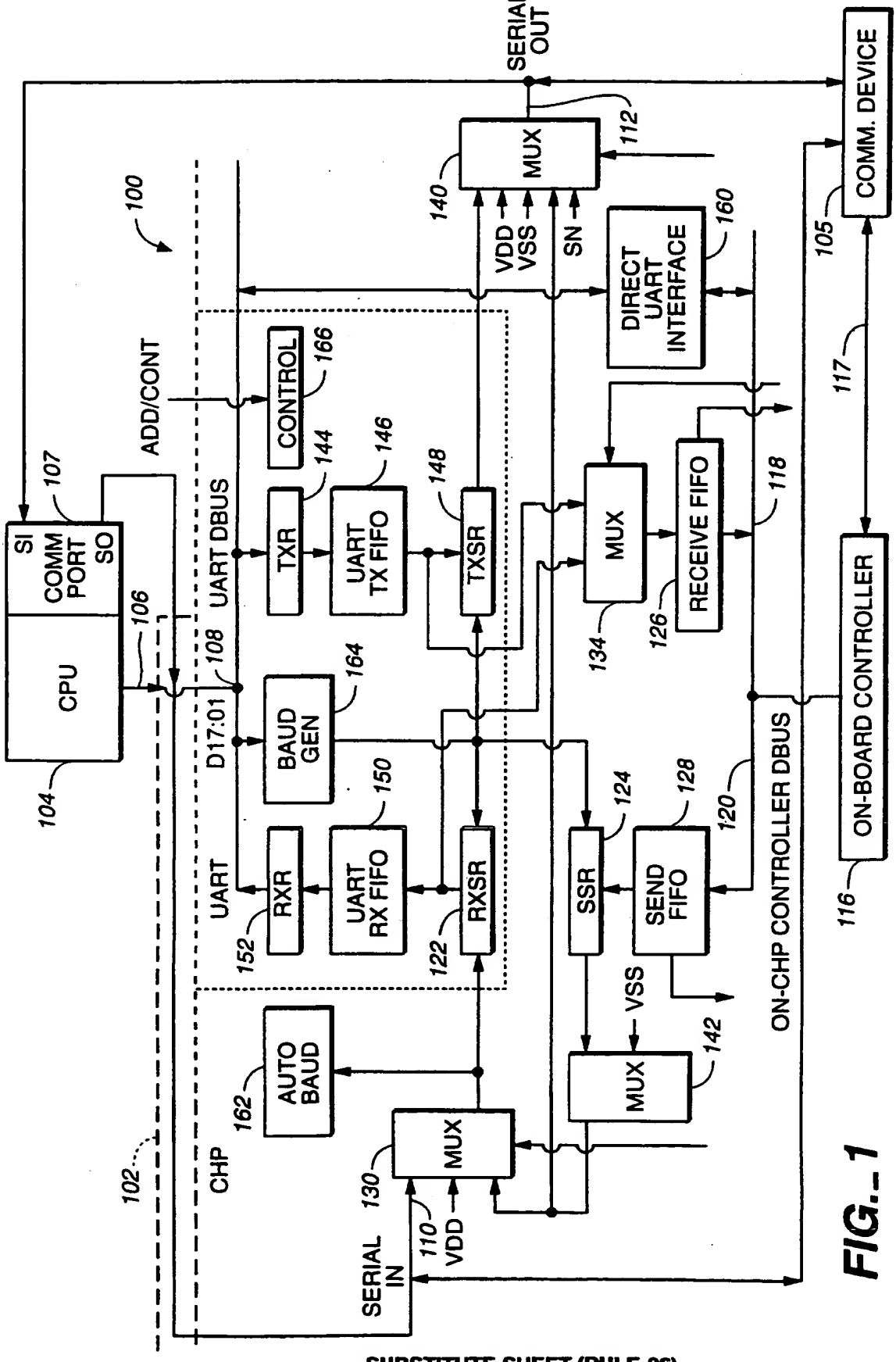
SERIAL OUT
COMM. DEVICE
105
MUX
112
140
VDD
VSS
SN
DIRECT UART INTERFACE
160
100
ADD/CONT
CONTROL
166
117
SI
COMM PORT
SO
107
UART DBUS
TXR
144
UART TX FIFO
146
TXSR
148
MUX
RECEIVE FIFO
118
CPU
106
108
134
126
104
D17:01
BAUD GEN
164
UART
RXR
152
UART RX FIFO
150
RXSR
122
SSR
124
SEND FIFO
128
120
ON-CHP CONTROLLER DBUS
ON-BOARD CONTROLLER
116
VSS
AUTO BAUD
162
MUX
142
CHP
102
MUX
130
SERIAL IN
110
VDD

FIG._1

INTERNATIONAL SEARCH REPORT

Inte. ..tional application No.
PCT/US96/15493

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G06F 13/12
US CL : 395/200.13

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/200.13, 200.01, 200.07, 200.12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS
search terms: computer?, communicat?, buffer?, asynchronous?, parallel?, serial?

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4,325,147 A (ROTHLAUF) 13 April 1982 (13.04.82), Col. 2 line 57 to Col. 3 line 4.	1-20
Y	US 5,140,679 A (MICHAEL) 18 August 1992 (18.08.92), Col. 2 line 44-60.	1-20
A	US 4,823,312 A (MICHAEL) 18 April 1989 (18.04.89), see entire document.	1-20
A	US 4,538,224 A (PETERSON) 27 August 1985 (27.08.85), see entire document.	1-20
A	US 4,264,954 A (BRIGGS ET AL) 28 April 1981 (28.04.81), see entire document.	1-20
A	US 3,772,656 A (SERRACCHIOLI ET AL) 13 November 1973 (13.11.73), see entire document.	1-20

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 OCTOBER 1996	07 NOV 1996
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer David Y. Eng Telephone No. (703) 306-9691

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